Attorney Docket No. 0553-0494

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of	)
Yoshinari HIGAKI et al.	)
Serial No.: 10/576,177	)
Filed: April 19, 2006	)
For: Semiconductor Device	)
Art Unit: 2874	)
Examiner: Tina Mei Seng Wong	)
Confirm No.: 7224	)

OK TO ENTER: /TW/

04/16/2009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE C (AFTER FINAL)

Sir:

Applicants have the following response to the Final Rejection of January 13, 2009.

Claim Rejections - 35 USC §103

In the Final Rejection, the Examiner rejects Claims 1-14 under 35 USC §103(a) as being unpatentable over Suzawa et al. (US 7,071,037). This rejection is respectfully traversed.

More specifically, in the rejection, the Examiner continues to contend that with regard to, for example, independent Claim 1, that Suzawa teaches a semiconductor device comprising a transparent conductive film (Col. 11) and a plurality of thin film transistors (Fig. 15) having a semiconductor thin film (1001 & 1002b) over a substrate having an insulating surface (1004) and an electrode or a

electrode or a wiring formed by stacking a first conductive layer (1002a) in contact with the semiconductor thin film and a second conductive layer (1003) on the first conductive layer wherein the first conductive layer has a larger width than the second conductive layer. The Examiner admits that Suzawa fails to disclose the transparent conductive film to be in contact with a part of the first conductive film extending from an end portion of the second conductive layer. The Examiner, however, contends that Suzawa teaches the transparent conductive film to be formed over the entire surface, and that although Suzawa does not explicitly teach the two films to be touching, the Examiner argues that it can be reasonably inferred from the embodiments disclosed by Suzawa that the two films are minimally in indirect optical/electrical contact with each other since each of the layers of the device work together to function. The Examiner then concludes that it would have been obvious at the time the invention was made to a person having ordinary skill in the art for the two films to be at least indirectly in optical/electrical contact with each other. Applicants respectfully disagreed.

In Applicants' prior response, Applicants explained that in Suzawa, reference numeral 1003 is a pixel electrode (see Col. 2) and corresponds more closely to a transparent conductive film of Claim 1 (i.e. a transparent pixel electrode) than the claimed second conductive film. If this is the case, then Suzawa does not disclose the claimed second conductive layer. If one were to argue that pixel electrode 1003 in Suzawa corresponds to the claimed second conductive layer, then there is no disclosure or suggestion in Suzawa of the claimed transparent conductive film. Therefore, the number of films (i.e. layers) disclosed in Suzawa is different than that claimed in independent Claim 1, and hence, Suzawa does not disclose or suggest all of the elements of Claim 1.

In response, in the Final Rejection, in the "Response To Arguments" section, the Examiner

argues "Applicant argues the pixel electrode (1003) more closely corresponds to the transparent conductive film as claimed and therefore, Suzawa et al does not teach enough layers. However, the Examiner disagrees. The claim language does not preclude the Examiner from interpreting the claim so that element 1003 is the second conductive layer and the transparent conductive film (discussed in Column 11 of Suzawa et al) as the transparent layer as claimed. The argument does not reflect the language." Applicants continue to disagree with this argument by the Examiner.

More specifically, Columns 10-11 in Suzawa (Embodiment Mode 2) describe the following steps:

1. A conductive film is formed on the entire surface of a substrate and is later etched to form a gate electrode through a first photolithography step.

2. Next, an insulating film is formed on the entire surface of the conductive film and later functions as a gate insulating film.

3. Then, a first amorphous semiconductor film, a second amorphous semiconductor film, and a conductive layer (i.e. a metal layer) are deposited on the insulating film. An unnecessary portion of these films are etched through a second photolithography step.

4. Next, a transparent conductive film is formed on the entire surface.

5. Thereafter, a part of the first amorphous semiconductor film, the second amorphous semiconductor film, the metal layer, and the transparent conductive film is **removed through a third photolithography step** to form source and drain regions of a gate electrode while forming a source wiring from the metal layer and **forming a pixel electrode from the transparent conductive film**.

Hence, the transparent conductive film formed on the entire surface and the pixel electrode in Suzawa are not different layers. Rather, the pixel electrode is formed from the transparent conductive film through the third photolithography step. Therefore, even if it were argued that the

pixel electrode (1003) in Suzawa corresponds to the claimed second conductive film, there is still no element in Suzawa which corresponds to the claimed transparent conductive film.

Therefore, independent Claim 1 is not disclosed or suggested by Suzawa. For similar, reasons, independent Claims 2-6 are also not disclosed or suggested by Suzawa. Accordingly, independent Claims 1-6 and those claims dependent thereon are patentable over Suzawa, and it is respectfully requested that this rejection be withdrawn.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee should be due for this response, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Date: April 13, 2009

Respectfully submitted,

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